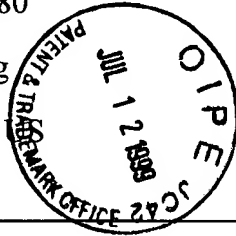


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mostafazadeh, Shahram; Smith, Joseph O.
Assignee: National Semiconductor Corporation
Title: LEAD FRAME DESIGN FOR INCREASED CHIP PINOUT
Serial No.: 09/054,380 Filed: April 2, 1998
Examiner: H. Duong Group Art Unit: 2822
Docket No.: NS-3856



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**INFORMATION DISCLOSURE STATEMENT WITH FEE
UNDER § 1.17(p)**

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents listed on the attached PTO form 1449 to the attention of the Examiner.

The document listed on sheet 1 of the attached PTO form 1449 is enclosed herewith.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

Please charge Deposit Account No. 19-2386 \$240.00 for the Information Disclosure Statement fee under 37 C.F.R. §1.17(p). The Commissioner is hereby authorized to charge

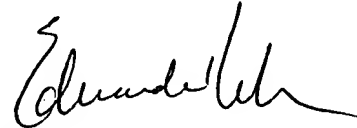
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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: ASSISTANT COMMISSIONER FOR PATENTS, Washington, D.C. 20231,

on July 8, 1999
Edward C. Kwok 7/8/99
Attorney for Applicant(s) Date of Signature

Respectfully submitted,



Edward C. Kwok
Attorney for Applicants
Reg. No. 33,938